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EXAMINER	
ARCOS, CAROLINE H	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/774,178	YEUNG ET AL.	
	Examiner	Art Unit	
	CAROLINE ARCOS	2195	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-50* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-50* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *04/11/2005, 07/25/2005 AND 01/24/2008*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-50 are pending for examination.

Specification

2. The abstract of the disclosure is objected to because the abstract contains a paragraph number and it contains more than 150 words. Correction is required. See MPEP § 608.01(b).

3. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75 (d)(1) and MPEP 608.01(o). Correction of the following is required: Claim 14, "a computer readable medium" is not disclosed in the specification to support the claimed limitation.

Claim Objections

4. Claim 33 is objected to because of the following informalities: Line 4, "the resource in the system is increased or decreased" has to be changed to "the resources in the system are increased or decreased" since there is a plurality of resources.

Appropriate correction is required.

Claim Rejections - 35 USC § 101

5. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

6. Claims 14-19 and 48-50 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

7. Claim 14 is rejected under 35 U.S.C. 101 because the claimed invention is directed to non- statutory subject matter. As per claim 14, the claimed "computer readable medium" is broad and can include both readable and storage medium, wherein computer- readable medium can include non-tangible medium. Claims 15-19 are rejected for similar reasons as discussed for their respective parent claims, as they fail to present any limitations that resolve the deficiencies of the claims from which they depend. Applicant is suggested to amend the claim to "a computer readable storage medium" that is covered by the published specification par. [0072].

8. Claim 48 is rejected under 35 U.S.C. 101 because the claimed invention is directed to an apparatus claims but appearing to be comprised of software alone without claiming associated computer hardware required for execution. For example, claim 48 recites a logic to monitor states of application, logic to monitor states of one or more threads and logic to adjust resource available, which are all software modules/functions. Software alone is directed to a non-statutory subject matter. Claims 49-50 are rejected for similar reasons as discussed for their respective parent claims, as they fail to present any limitations that resolve the deficiencies of the claims from which they depend.

Claim Rejections - 35 USC § 112

9. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

10. Claims 1-19, 29, 37, 39 and 46 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

a. The following terms lacks antecedent basis:

i. The state of the one or more threads – claim 1.

b. The claim language in the following claims is not clearly understood:

i. As per claim 1, line 5, it is not clearly understood what are the criteria of dispatching of one or more threads and how the controlling of the dispatching is done.

ii. As per claim 3, lines 2, it is not clearly understood what are the criteria for delaying a ready- to be- dispatched activity from being dispatched.

iii. As per claim 5, lines 4, it is not clearly understood whether "resources" are the same resources referred to in claim 1(i.e. if they are the same resources, it should be referred to as said resource".)

iv. As per claim 14, lines 7, it is unclear what are the criteria of dispatching of one or more threads in the system? and how the controlling of the dispatching is done.

v. As per claim 15, line 2, it is not clearly understood what are the criteria for delaying a ready- to be- dispatched activity from being dispatched.

vi. As per claim 29, lines 2-3, it is unclear what are the criteria for changing the state of the threads from ready to queued state.

vii. As per claim 37, lines 2-3, it is not clearly understood what are the criteria of placing a thread from a ready state to a delay state. It is not clearly understood whether " a ready to be dispatched state" and " a delay from being dispatched state" as the same as the ones referred to in claim 36 (i.e. if they are the same they should be referred to as " said ready to be dispatched state" and " said delay from being dispatched state")

viii. As per claim 39, line 12, it is not clearly understood what are the criteria of dispatching of one or more threads and how the controlling of the dispatching is done.

ix. As per claim 46, lines 2, it is uncertain whether "a thread from a ready state to a queued state" is the same as "a thread from a ready state to a queued state" referred to in claim 45 (if it is the same, it should be referred to as "said thread from said ready state to said queued state").

Claim Rejections - 35 USC § 102

11. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

12. Claims 20-21, 26-28 and 34 are rejected under 35 U.S.C. 102 (a) as being anticipated by Zaccarin et al. (US 2003/0115428 A1).

13. As per claim 20, Zaccarin teaches a method, comprising:

managing resources in a system by monitoring buffer fullness levels of one or more buffers used by an application running in the system and by coordinating dispatch of threads in the system (abs., lines 9-12; col. 2, lines 29-32; col. 2, lines 62-66; col. 12, lines 18-28; wherein changing the rate of transmission of data is coordinating dispatch of threads in the system).

14. As per claim 21, Zaccarin teaches said monitoring the buffer fullness levels of the one or more buffers includes monitoring buffer level of each of the one or more buffers to determine buffer overflow or underflow conditions (par. [0015], lines 4-16; par. [0017], lines 4-15).

15. As per claim 26, Zaccarin teaches that when the buffer fullness levels of all of the buffers reach a critical stage, the resources in the system are adjusted (par. [0014]; par. [0015]; par. [0016]; par. [0017]; wherein the buffer reaching low or high level is a critical stage as claimed).

16. As per claim 27, Zaccarin teaches a computer readable medium containing executable instructions which, when executed in a processing system, causes the processing system to perform a method comprising: managing resources in a system by monitoring buffer fullness levels of one or more buffers used by an application running in the system and by coordinating dispatch of threads in the system (par. [0013], lines 5-7; (par. [0013], lines 11-12; par. [0014],

lines 1-23; par. [0015]; par. [0017], lines 4-15; par. [0021]).

17. As per claim 28, Zaccarin teaches wherein said monitoring the buffer fullness levels includes monitoring for buffer overflow or underflow conditions, and correspondingly increasing or decreasing the resources in the system to avoid the buffer overflow or underflow conditions par. [0013], lines 5-7; (par. [0013], lines 11-12; par. [0014], lines 1-23; par. [0015]; par. [0017], lines 4-15; par. [0021]).

18. As per claim 34, Zaccarin teaches a method, comprising:

monitoring a state of an application running in a system,

wherein said monitoring the state of the application includes monitoring buffer fullness levels of one or more buffers associated with the application (abs., lines 9-12; col. 2, lines 29-32; col. 2, lines 62-66; col. 12, lines 18-28; par. [0015], lines 4-16; par. [0017], lines 4-15); and

managing resources in the system based on the state of the application (par. [0014]; par. [0015]; par. [0017]).

Claim Rejections - 35 USC § 103

19. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

20. Claims 1, 5-9, 11-14 and 16-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Paul et al. (US 7,185,070 B2), in view of Zaccarin et al. (US 2003/0115428 A1)

21. As per claim 1, Paul teaches the invention substantially as claimed including a method, comprising:

monitoring a state of an application running in a system, wherein said monitoring the state of the application includes monitoring one or more buffers associated with the application (abs., lines 9-12; col. 2, lines 29-32; col. 2, lines 62-66; col. 12, lines 18-28);

managing resources in the system based at least on the state of the application and the state of the one or more threads in the system (col. 11, lines 6-12; col. 12, lines 32-49).

22. Paul doesn't explicitly teach controlling dispatch of one or more threads in the system, and wherein at least one thread in the system is associated with the application. However, Zaccarin teaches controlling dispatch of one or more threads in the system, and wherein at least one thread in the system is associated with the application (par. [0013], lines 5-7; par. [0014], lines 1-23; par. [0021]).

23. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine from Paul and Zaccarin because Zaccarin teaching of controlling the transmission rate of data (threads) associated with the application would improve Paul system performance and efficiency in reducing overall power consumption and improve system

resource usage.

24. As per claim 5, Zaccarin teaches monitoring a machine state of the system, wherein said monitoring the machine state includes: increasing or decreasing the resources available in the system based on the state of the application and the state of the one or more threads in the system (par. [0013], lines 11-12; par. [0014], lines 9-23).

25. The combined teaching of Paul and Zaccarin doesn't explicitly teach that determining resources available in the system. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to conclude from Zaccarin teaching of monitoring buffer levels and control it through changing the frequency and the voltage of the processor is that determine availability of resource in the system (buffer and processor) and using them in balancing the system and improve system energy consumption.

26. As per claim 6, Zaccarin teaches that the resources include configurable hardware components (par. [0019], lines 4-9; par. [0021], lines 9-13).

27. As per claim 7, Zaccarin teaches the configurable hardware components include one or more processors, hardware buffers, memory, cache, arithmetic logic unit (ALU), and registers in the system (par. [0019], lines 4-9; par. [0021], lines 9-13).

28. As per claim 8, Zaccarin teaches said increasing or decreasing the resources available in the system includes configuring the frequencies applied to at least the one or more processors in the system (par. [0015], lines 8-11).

29. As per claim 9, Zaccarin teaches said increasing or decreasing the resources available in the system includes configuring the voltages applied to at least the one or more processors in the system (par. [0015], lines 8-11).

30. As per claim 11, Zaccarin teaches said monitoring the one or more buffers associated with the application includes monitoring buffer fullness levels of the one or more buffers (par. [0013], lines 11-12; par. [0014], lines 10-23; par. [0015], lines 8-16; par. [0016], lines 10-12; par. [0018]).

31. As per claim 12, Zaccarin teaches said monitoring the buffer fullness levels includes, for each buffer associated with the application, comparing a buffer level with predetermined buffer fullness levels, wherein the predetermined buffer fullness levels include a high level mark and a low level mark (par. [0015], lines 8-16; Par. [0017]; par. [0018]).

32. As per claim 13, Zaccarin teaches said comparing is to determine buffer overflow and buffer underflow conditions (par. [0015], lines 4-16; par. [0017], lines 4-15).

33. As per claim 14, Paul teaches a computer readable medium containing executable instructions which, when executed in a processing system, causes the processing system to perform a method comprising:

monitoring a state of an application running in a system, wherein said monitoring the state of the application includes monitoring buffer fullness levels of one or more buffers associated with the application (abs., lines 9-12; col. 2, lines 29-32; col. 2, lines 62-66; col. 12, lines 18-28); and

managing resources in the system based at least on the state of the application and the state of the one or more threads in the system(col. 11, lines 6-12; col. 12, lines 32-49; wherein the data transmitted is one or more threads).

34. Paul doesn't explicitly teach controlling dispatch of one or more threads in the system, and wherein at least one thread in the system is associated with the application. However, Zaccarin teaches controlling dispatch of one or more threads in the system, and wherein at least one thread in the system is associated with the application (par. [0013], lines 5-7; par. [0014], lines 1-23; wherein the data transmitted by the application is the one or more thread associated by with the application).

35. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine from Paul and Zaccarin because Zaccarin teaching of controlling the transmission rate of data (threads) associated with the application would improve Paul system performance and efficiency in reducing overall power consumption and improve system

resource usage.

36. As per claim 16, it is the computer readable medium of the method claim 5. Therefore it is rejected under the same rational.

37. As per claim 17, it is the computer readable medium of the method claim 6. Therefore it is rejected under the same rational.

38. As per claim 18, Zaccarin teaches said increasing or decreasing the resources available in the system includes configuring the frequencies and/or the voltages applied to at least the one or more processors in the system (par. [0015], lines 8-11).

39. As per claim 19, Zaccarin teaches said monitoring the buffer fullness levels includes, for each buffer associated with the application, comparing a buffer level with predetermined buffer fullness levels, wherein the predetermined buffer fullness levels include a high level mark and a low level mark (par. [0013], lines 11-12; par. [0014], lines 10-23; par. [0015], lines 8-16; par. [0016], lines 10-12; par. [0017]; par. [0018]).

40. Claims 2-4 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Paul et al. (US 7,185,070 B2), in view of Zaccarin et al. (US 2003/0115428 A1) as applied to claims 1 and 14 above, and further in view of Kling et al. (US 6,662,203 B1).

41. As per claim 2, Zaccarin teaches a thread includes one or more activities (par. [0021], lines 1-20).

42. The combined teaching of Paul and Zaccarin doesn't explicitly teach that a thread includes one or more activities, and wherein said controlling the dispatch of the one or more threads in the system includes assessing execution readiness of the one or more activities.

43. However, Kling teaches a thread includes one or more activities, and wherein said controlling the dispatch of the one or more threads in the system includes assessing execution readiness of the one or more activities (abs; col. 9, lines 35-67; col. 10, lines 1-9; fig. 5, 77).

44. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Paul, Zaccarin and kling because Kling teaching of accessing readiness of the one or more activities improve system dispatching techniques and increase efficiency in dispatching technique of the system since one would only be dispatching ready activities only which improve the performance of the system.

45. As per claim 3, Kling teaches said controlling the dispatch of the one or more threads in the system includes delaying a ready-to-be-dispatched activity from being dispatched (abs.; col. 1, lines 66- col. 2, lines 1-16; col. Col. 3, lines 58-col. 4, lines 1-24; col. 9, lines 38-col. 10, lines 1-15).

46. As per claim 4, Zaccarin teaches the first and second activities are from one or more applications (par. [0012]; par. [0021]).

47. The combined teaching of Paul and Zaccarin doesn't explicitly teach that a first activity is delayed from being dispatched to wait for a second activity to be ready so that both the first and second activities can be dispatched together. However, Kling teaches a first activity is delayed from being dispatched to wait for a second activity to be ready so that both the first and second activities can be dispatched together.

48. As per claim 15, it is the computer readable medium of the method claim 3. Therefore it is rejected under the same rational.

49. Claim 10 rejected under 35 U.S.C. 103(a) as being unpatentable over Paul et al. (US 7,185,070 B2), in view of Zaccarin et al. (US 2003/0115428 A1) as applied to claim 7 above and further in view of Jain et al. (US 2002/0188884 A1).

50. As per claim 10, the combined teaching of Paul and Zaccarin doesn't explicitly teach that said increasing or decreasing the resources in the system includes powering on or powering off at least a portion of circuitry in the system. However, Jain teaches said increasing or decreasing the resources in the system includes powering on or powering off at least a portion of circuitry in the system (par. [0040]; claim 16).

51. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Paul, Zaccarin and Jain because Jain teaching of said increasing or decreasing the resources in the system includes powering on or powering off at least a portion of circuitry in the system would improve system energy consumption and increase efficiency.

52. Claims 22-25, 29-31, 33, 35-38 and 48-50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zaccarin et al. (US 2003/0115428 A1) and in view of Kling et al. (US 6,662,203 B1).

53. As per claim 22, Zaccarin doesn't explicitly teach that said coordinating the dispatch of the threads in the system is performed to increase overlap in threads execution. However, Kling teaches that said coordinating the dispatch of the threads in the system is performed to increase overlap in threads execution (col. 2, lines 10-16).

54. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Zaccarin and Kling because Kling teaching of controlling dispatch of the threads improve system performance by processing several threads at once.

55. As per claim 23, Kling teaches increasing the overlap in the threads execution includes changing a thread from a ready state to a queued state (abs.; col. 1, lines 66- col. 2, lines 1-16; col. Col. 3, lines 58-col. 4, lines 1-24; col. 9, lines 38-col. 10, lines 1-15).

56. As per claim 24, Kling teaches the thread remains in the queued state until there is another thread in the ready state such that both threads can be dispatched together (abs.; col. 1, lines 66- col. 2, lines 1-16; col. Col. 3, lines 58-col. 4, lines 1-24; col. 9, lines 38-col. 10, lines 1-15).

57. As per claim 25, Zaccarin teaches that said coordinating the dispatch of the threads in the system includes the buffer fullness levels of all of the buffers indicate a potential overflow condition; the resources in the system are increased (par. [0015], lines 8-16).

58. Zaccarin doesn't explicitly teach that said coordinating the dispatch of the threads in the system includes determining threads dependency, and wherein when there is dependency between a current thread and a next thread of the application.

59. However, Kling teaches aid coordinating the dispatch of the threads in the system includes determining threads dependency, and wherein when there is dependency between a current thread and a next thread of the application (col. 6, lines 38-54; col. 7, lines 35-65).

60. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Zaccarin and Kling because Kling teaching of determining threads dependency, and wherein when there is dependency between a current thread and a next thread of the application would improve system efficiency and would allow system fine tuning to solve the issue.

61. As per claim 29, Zaccarin doesn't explicitly teach that said coordinating the dispatch of the threads in the system includes changing a thread from a ready state to a queued state and dispatching threads to increase execution overlap. However, Kling teaches aid coordinating the dispatch of the threads in the system includes changing a thread from a ready state to a queued state and dispatching threads to increase execution overlap.

62. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Zaccarin and kling because Kling teaching of changing a thread from a ready state to a queued state and dispatching threads to increase execution overlap improve system dispatching techniques and increase efficiency in dispatching technique and use of system resource since one would be dispatching multiple threads at once which improve the performance of the system.

63. As per claim 30, Zaccarin teaches a method, comprising:

monitoring states of one or more threads in a system (par. [0013]; par. [0014] ;

managing resources in the system based at least on the states of the one or more threads in the system, wherein the resources include configurable hardware components in the system ([0014]; par. [0015]; par. [0017]; par. [0021]).

64. Zaccarin doesn't explicitly teach that said monitoring the states of the one or more threads includes monitoring readiness to dispatch of the one or more threads. However, Kling teaches that said monitoring the states of the one or more threads includes monitoring readiness

to dispatch of the one or more threads (abs; col. 9, lines 35-67; col. 10, lines 1-9; fig. 5, 77).

65. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Zaccarin and kling because Kling teaching of monitoring the states of the one or more threads includes monitoring readiness to dispatch of the one or more threads would improve system dispatching techniques and increase efficiency in dispatching technique of the system since one would only be dispatching ready threads only which improve the performance of the system..

66. As per claim 31, Zaccarin teaches said managing the resources in the system includes configuring the frequencies and/or voltages applied to at least one or more processors in the system (par. [0015], lines 8-11).

67. As per claim 33, Zaccarin teaches managing state of an application running in the system, wherein the state of the application includes buffer fullness levels of one or more buffers used by the application ;

the resources in the system is increased or decreased based on the state of the application (par. [0013], lines 11-12; par. [0014], lines 9-23).

68. As per claim 35, Zaccarin doesn't explicitly teach that managing execution readiness of one or more threads in the system, and wherein said managing the resources is further based on

the execution readiness of at least a thread associated with the application.

69. However, Kling teaches managing execution readiness of one or more threads in the system, and wherein said managing the resources is further based on the execution readiness of at least a thread (abs; col. 9, lines 35-67; col. 10, lines 1-9; fig. 5, 77).

70. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Zaccarin and kling because Kling teaching of managing execution readiness of one or more threads in the system, and wherein said managing the resources is further based on the execution readiness of at least a thread improve system dispatching techniques and increase efficiency in dispatching technique of the system since one would only be dispatching ready threads only which improve the performance of the system.

71. The combined teaching of Zaccarin and kling doesn't explicitly teach that said thread associated with the application. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to conclude from Zaccarin and kling that the threads/ jobs is associated with one or more application which is obvious that a thread is associated with the application as claimed.

72. As per claim 36, Kling teaches the execution readiness includes a ready-to- be-dispatched state and a delay-from-being-dispatched state (abs.; col. 1, lines 66- col. 2, lines 1-16; col. Col.

3, lines 58-col. 4, lines 1-24; col. 9, lines 38-col. 10, lines 1-15; fig. 5).

73. As per claim 37, Kling teaches said managing the execution readiness of the one or more threads in the system includes placing a thread from a ready-to- be-dispatched state into a delay-from-being-dispatched state (abs.; col. 1, lines 66- col. 2, lines 1-16; col. Col. 3, lines 58-col. 4, lines 1-24; col. 9, lines 38-col. 10, lines 1-15; fig. 5).

74. As per claim 38, Zaccarin teaches that said monitoring the buffer fullness levels of the one or more buffers includes: determining a potential buffer underflow or overflow condition; and configuring one or more components in the system to change resources available in the system to avoid the potential buffer underflow or overflow condition (par. [0013], lines 11-12; par. [0014], lines 10-23; par. [0015], lines 8-16; par. [0016], lines 10-12; par. [0017]; par. [0018]).

75. As per claim 48. Zaccarin teaches an apparatus, comprising:

logic to monitor states of an application running in a system, the states of the application including buffer fullness levels of one or more buffers used by the application (abs., lines 9-12; col. 2, lines 29-32; col. 2, lines 62-66; col. 12, lines 18-28; par. [0015], lines 4-16; par. [0017], lines 4-15);

logic to adjust resources available in the system depending on the state of the application and/or the states of the one or more threads in the system (par. [0014]; par. [0015];

par. [0016]).

76. Zaccarin doesn't explicitly teach logic to monitor states of one or more threads in the system for execution readiness. However, Kling teaches logic to monitor states of one or more threads in the system for execution readiness (abs; col. 9, lines 35-67; col. 10, lines 1-9; fig. 5, 77).

77. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Zaccarin and Kling because Kling teaching of monitoring the execution readiness of one or more thread would improve Zaccarin system performance and dispatching techniques by knowing that one or more threads are ready to be executed , one would be able to take the steps necessary to dispatch them.

78. As per claim 49, Kling teach logic to change the execution readiness of a thread from a ready state to a queued state (abs.; col. 1, lines 66- col. 2, lines 1-16; col. Col. 3, lines 58-col. 4, lines 1-24; col. 9, lines 38-col. 10, lines 1-15; fig. 5).

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79. The combined teaching of Zaccarin and Kling doesn't explicitly teach that the change in state is when it is determined that there is no other thread running or ready to be dispatched.

80. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to conclude from the combined teaching and especially Kling teaching that

the ready threads are moved to wait queue until the batch is complete to be dispatched so it would have been obvious that the first thread in the ready queue is moved to the wait queue until other ready threads becomes ready and join the first thread in the wait queue, when they will be dispatched.

81. As per claim 50, Zaccarin teaches that the logic to adjust the available resources in the system includes logic to determine if the buffer fullness levels of one or more buffers are in a critical stage (par.[0015]; par. [0017]).

82. Claim 32 is rejected under 35 U.S.C. 103(a) as being unpatentable over Zaccarin et al. (US 2003/0115428 A1), in view of Kling et al. (US 6,662,203 B1) as applied to claim 30 above and further in view of Jain et al. (US 2002/0188884 A1).

83. As per claim 32, the combined teaching of Zaccarin and Kling doesn't explicitly teach managing the resources in the system further includes powering on or powering off a portion of circuitry in the system. However, Jain teaches said managing the resources in the system further includes powering on or powering off a portion of circuitry in the system. (par. [0040]; claim 16).

84. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Zaccarin and Jain because Jain teaching of said increasing or decreasing

the resources in the system includes powering on or powering off at least a portion of circuitry in the system would improve system energy consumption and increase efficiency.

85. Claims 39 and 41-43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zaccarin et al. (US 2003/0115428 A1), in view of Jain et al. (US 2002/0188884 A1).

86. As per claim 39, Zaccarin teaches a system, comprising:

a memory (fig. 4; 42);

processor (fig. 4, 56);

monitor a state of an application running in a system, wherein said monitoring the state of the application includes monitoring buffer fullness levels of one or more buffers associated with the application (par. [0013]; par. [0014]

control dispatch of one or more threads in the system, and wherein at least one thread in the system is associated with the application; and manage resources in the system based at least on the state of the application and the state of the one or more threads in the system (par. [0014]; par. [0015]; par. [0021]).

87. Zaccarin doesn't explicitly teach a memory to store data and instructions;

a processor coupled to said memory on a bus, said processor operable to perform instructions, said processor comprising:

a bus unit to receive a sequence of instructions from said memory;

an execution unit coupled to said bus unit, said execution unit to execute said sequence of

instructions.

88. However, Jain teaches teach a memory to store data and instructions;

a processor coupled to said memory on a bus, said processor operable to perform instructions, said processor comprising:

a bus unit to receive a sequence of instructions from said memory;

an execution unit coupled to said bus unit, said execution unit to execute said sequence of instructions (fig. 1; par. [0026]; par. [0027]; par. [0028]; [par. [0031]).

89. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Zaccarin and Jain because Jain teaching explicitly explain the hardware layout and the hardware structure used by Zaccarin system, since it is obvious to one of ordinary skill in the art at the time the invention was made that any system needs a a memory for storage of data and any instruction execution and a processor for execution and a bus that connect all the hardware together for communication purpose.

90. As per claim 41, Zaccarin teaches that said execution unit to monitor a machine state of the system, wherein said monitoring the machine state includes: increasing or decreasing the resources available in the system based on the state of the application and the state of the one or more threads in the system (par. [0014]; par. [0015]; par. [0017]).

91. The combined teaching of Zaccarin and Jain doesn't explicitly teach that determining resources available in the system. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to conclude from Zaccarin teaching of monitoring applications state by monitoring buffers levels and since Zaccarin monitoring the levels of the buffer, it would have been obvious to one of ordinary skill in the art to determine resources available as claimed since the resource is increased or decreased.

92. As per claim 42, Zaccarin teaches that the resources include configurable hardware components (fig. 4, 54, 56; par. [0013]).

93. As per claim 43, Zaccarin teaches said increasing or decreasing the resources available in the system includes configuring the frequencies and the voltages applied to at least the one or more processors in the system (par. [0014]; par. [0015]).

94. Claim 40 is rejected under 35 U.S.C. 103(a) as being unpatentable over Zaccarin et al. (US 2003/0115428 A1), in view of Jain et al. (US 2002/0188884 A1) applied to claim 39 above and further in view of Kling et al. (US 6,662,203 B1).

95. As per claim 40, the combined teaching of Zaccarin and Jain doesn't explicitly teach that said controlling the dispatch of the one or more threads in the system includes delaying a ready-to-be-dispatched thread from being dispatched.

96. However, Kling teaches said controlling the dispatch of the one or more threads in the system includes delaying a ready-to-be-dispatched thread from being dispatched(abs.; col. 1, lines 66- col. 2, lines 1-16; col. Col. 3, lines 58-col. 4, lines 1-24; col. 9, lines 38-col. 10, lines 1-15; fig. 5).

97. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Zaccarin, Jain and ling since Kling teaching of delaying a ready-to-be-dispatched thread from being dispatched would improve system throughput and increase efficiency of system resource usage.

98. Claims 44-47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zaccarin et al. (US 2003/0115428 A1), in view of Kling et al. (US 6,662,203 B1) and further in view of Peter et al. (US 5,668,993).

99. As per claim 44, Zaccarin teaches a system, comprising:

processor (fig. 4, 56);

a resource manager coupled to the multi-threading processor (fig. 4);

the resource manager is to monitor states of an application running in the system, the states of the application including buffer fullness levels of one or more buffers used by the application, wherein the resource manager is to increase or decrease resources available in the system depending on the state of the application and/or the states of the one or more threads in

the system (par. [0013]; par. [0014]; par. [0015]; par. [0017]; par. [0021]).

100. Zaccarin doesn't explicitly teach a multi-threading processor; and
the resource manager is to further monitor states of one or more threads in the system for execution readiness.

101. However, kling teaches the resource manager is to further monitor states of one or more threads in the system for execution readiness (abs.; col. 1, lines 66- col. 2, lines 1-16; col. Col. 3, lines 58-col. 4, lines 1-24; col. 9, lines 38-col. 10, lines 1-15; fig. 5).

102. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Zaccarin and Kling because Kling teaching of monitor states of one or more threads in the system for execution readiness would improve dispatching and scheduling techniques and system performance by monitoring ready thread to dispatch them.

103. The combined teaching doesn't explicitly teach that the processor is a multi-threaded processor. However, Peter teaches that the processor is multi-threaded processor (col. 5, lines 35-40; col. 9, lines 50-56).

104. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Zaccarin, kling and Peter because Peter teaching of multithreaded

processor would improve system performance and throughput.

105. As per claim 45, Kling teaches that wherein the resource manager is to change the execution readiness of a thread from a ready state to a queued state to increase subsequent thread execution overlap with execution of another thread (col. 2, lines 10-16).

106. As per claim 46, Kling teaches change the execution readiness of a thread from a ready state to a queued state (abs.; col. 1, lines 66- col. 2, lines 1-16; col. Col. 3, lines 58-col. 4, lines 1-24; col. 9, lines 38-col. 10, lines 1-15).

107. The combined teaching of Zaccarin, Kling and Peter doesn't explicitly teach that the change is to increase subsequent system idle time when there is no thread execution. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to conclude from Kling teaching of batch system and changing from ready to queued state that beside increasing the efficiency in using the system resource, it is increasing subsequent system idle time when there is no thread execution which improve the system throughput by processing the threads in a parallel at once..

108. As per claim 47, Zaccarin teaches the resource manager is to increase or decrease the resources available in the system to avoid buffer underflow or overflow conditions to occur to the one or more buffers (par. [0013]; par. [0014]; par. [0015]; par. [0017]).

Conclusion

107. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US 5133077 A teaches Data processor having multiple execution units for processing plural classs of instructions in parallel.

US 6493741 B1 teaches Method and apparatus to quiesce a portion of a simultaneous multithreaded central processing unit.

US 20040083478 A1 teaches Apparatus and method for reducing power consumption on simultaneous multi-threading systems.

US 20010043353 A1 teaches information processing apparatus and mode control for controlling power consumption.

EP 636985 A1 teaches Process monitoring in a multiprocessing server.

EP 1395000 A1 teaches a method of transmitting data streams dependent on the monitored state of the client application buffer.

US 20040215668 A1 teaches Methods and apparatus to manage a cache memory.

108. Any inquiry concerning this communication or earlier communications from the examiner should be directed to CAROLINE ARCOS whose telephone number is (571)270-3151. The examiner can normally be reached on Monday-Thursday 7:00 AM to 5:30 PM.

109. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on 571-272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

110. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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